verilog for advanced digital design

verilog for advanced digital design is a critical topic in modern electronics and computer engineering, enabling the creation and verification of complex digital systems. This hardware description language (HDL) allows engineers to model, simulate, and synthesize digital circuits at various levels of abstraction. With the increasing complexity of integrated circuits and system-on-chip (SoC) designs, mastering Verilog for advanced digital design is essential for efficient and reliable hardware development. This article explores the key concepts, techniques, and best practices involved in using Verilog to implement sophisticated digital logic, including timing analysis, design hierarchy, and verification methodologies. Additionally, it covers the integration of behavioral and structural modeling for high-performance designs. The following sections provide a comprehensive overview of Verilog's role in advanced digital design workflows and its impact on modern hardware engineering.

- Fundamentals of Verilog in Advanced Digital Design
- Advanced Modeling Techniques in Verilog
- Verification and Testing Strategies
- Timing and Performance Optimization
- Design Hierarchy and Modularization
- Integration with Modern Design Flows

Fundamentals of Verilog in Advanced Digital Design

Understanding the fundamentals of Verilog is the foundation for leveraging this HDL in advanced digital design projects. Verilog provides a syntax and semantic framework that enables designers to describe hardware behavior, structure, and timing. It supports multiple abstraction levels, from gate-level netlists to high-level behavioral descriptions, making it versatile for complex design tasks. Key elements include modules, ports, data types, operators, and procedural blocks essential for creating synthesizable and testable hardware models.

Verilog Syntax and Core Constructs

The core syntax of Verilog revolves around modules that encapsulate hardware

components. Modules define input, output, and bidirectional ports, which connect to other modules or external signals. Inside modules, designers use continuous assignments for combinational logic and procedural blocks such as *always* and *initial* for sequential and initialization logic. Data types like *reg* and *wire* define signal storage and connectivity, while operators facilitate arithmetic, logical, and bitwise operations.

Synthesis and Simulation in Verilog

Verilog is designed for both simulation and synthesis, enabling designers to verify functionality before hardware implementation. Simulation tools interpret Verilog code to model circuit behavior over time, allowing detection of logical errors and timing violations. Synthesis tools convert Verilog descriptions into gate-level netlists compatible with target hardware technologies such as FPGAs and ASICs. Understanding the synthesis constraints and coding styles that ensure synthesizability is crucial for advanced digital design.

Advanced Modeling Techniques in Verilog

Advanced digital design often requires sophisticated modeling techniques to handle complex functionalities and optimize resource utilization. Verilog supports behavioral, structural, and dataflow modeling styles, which can be combined to create modular, reusable, and efficient designs. These modeling approaches help in representing intricate logic, control flows, and data processing units in a manageable way.

Behavioral Modeling for Complex Control Logic

Behavioral modeling in Verilog uses procedural blocks to describe how hardware behaves in response to input signals or clock events. This technique is ideal for implementing finite state machines (FSMs), arithmetic algorithms, and control units. Behavioral code allows for abstraction from gate-level details, focusing on algorithmic descriptions that synthesis tools translate into hardware structures.

Structural Modeling and Hierarchical Design

Structural modeling involves instantiating and interconnecting lower-level modules to build complex hardware systems. This hierarchical approach facilitates design reuse, improves readability, and simplifies debugging. By defining clear module interfaces and encapsulating functionality, structural modeling supports scalable and maintainable digital designs.

Dataflow Modeling and Continuous Assignments

Dataflow modeling uses continuous assignments and operators to describe combinational logic succinctly. This style is efficient for arithmetic operations, multiplexers, and combinational circuits where outputs are directly derived from inputs without sequential elements. Combining dataflow with behavioral and structural styles enhances design flexibility.

Verification and Testing Strategies

Verification is a critical phase in advanced digital design using Verilog to ensure that the design meets functional and timing requirements before fabrication or deployment. Effective testing strategies leverage simulation, testbenches, assertions, and formal verification techniques to detect and correct design flaws early.

Developing Testbenches in Verilog

Testbenches are specialized Verilog modules that generate stimulus and monitor outputs of the design under test (DUT). They simulate real-world operating conditions and provide automated verification environments. Writing comprehensive testbenches with stimulus generators, checkers, and scoreboards ensures robust testing of all design scenarios.

Assertions and Coverage Metrics

Assertions provide a mechanism to specify expected properties and behaviors within the Verilog code, enabling dynamic checking during simulation. Coupled with coverage metrics, assertions help identify untested design regions and improve verification completeness. These tools are essential for thorough verification in advanced digital design projects.

Formal Verification Techniques

Formal verification uses mathematical methods to prove the correctness of Verilog designs against specified properties without exhaustive simulation. This approach is particularly valuable for safety-critical systems and complex control logic, ensuring design integrity through rigorous proof techniques.

Timing and Performance Optimization

Timing and performance are paramount concerns in advanced digital design, where clock frequency, latency, and power consumption directly impact system effectiveness. Verilog offers constructs and methodologies to analyze and optimize timing behavior, ensuring reliable operation at target performance levels.

Clock Domain Management

Managing multiple clock domains and asynchronous interfaces is a common challenge in advanced designs. Verilog supports techniques such as clock domain crossing (CDC) synchronization and metastability mitigation to maintain data integrity and timing closure across varying clock signals.

Timing Constraints and Static Timing Analysis

Timing constraints specify the desired clock frequencies, setup and hold times, and input/output delays for synthesis and place-and-route tools. Static timing analysis (STA) verifies these constraints against the synthesized design, identifying critical paths and potential timing violations. Proper constraint definition in Verilog projects is essential for achieving timing closure.

Optimizing Resource Utilization

Advanced Verilog design involves optimizing logic utilization, power consumption, and area. Techniques include pipelining, resource sharing, and clock gating. These optimizations improve throughput and efficiency while adhering to design specifications and physical limitations.

Design Hierarchy and Modularization

Hierarchical design and modularization are fundamental practices in managing the complexity of advanced digital systems. Verilog’s modular structure encourages the decomposition of large designs into smaller, reusable components that simplify development, testing, and maintenance.

Module Instantiation and Parameterization

Modules can be instantiated multiple times with different parameters, allowing designers to create flexible and configurable components. Parameterization enhances code reuse and adaptability, enabling the same module to serve diverse functions in the design.

Interface Abstraction and Signal Encapsulation

Abstracting interfaces and encapsulating signals within modules improve design clarity and reduce errors. Using well-defined input/output ports and internal signals ensures clean communication between modules and supports hierarchical verification.

Design Reuse and IP Integration

Modular design facilitates the integration of intellectual property (IP) cores and third-party components. Verilog supports standard interfaces and protocols, enabling seamless incorporation of reusable blocks and accelerating the design cycle.

Integration with Modern Design Flows

Verilog for advanced digital design is integral to contemporary electronic design automation (EDA) flows that combine synthesis, simulation, verification, and implementation tools. Its compatibility with industry standards and methodologies enables efficient development of complex digital systems.

FPGA and ASIC Design Flows

Verilog is widely used in both FPGA and ASIC design flows, where designers write HDL code that is synthesized and mapped onto physical devices. The ability to simulate, synthesize, and verify within a unified environment streamlines the design process and reduces time to market.

Integration with High-Level Synthesis (HLS)

High-Level Synthesis tools translate algorithms written in high-level languages into Verilog or other HDLs. This integration allows designers to leverage algorithmic descriptions while retaining detailed control over hardware implementation, combining productivity with performance.

Use of Verification Methodologies

Modern verification methodologies such as Universal Verification Methodology (UVM) and SystemVerilog extensions complement Verilog designs by providing standardized, reusable testbench architectures. These methodologies enhance the verification process for complex

designs, improving coverage and debug capabilities.

- Master core Verilog syntax and semantics for effective hardware description.
- Employ behavioral, structural, and dataflow modeling to capture complex designs.
- Develop comprehensive testbenches leveraging assertions and formal methods.
- Apply timing constraints and optimize performance through analysis and design techniques.
- Use hierarchical design and parameterization for modular, reusable hardware components.
- Integrate Verilog into modern EDA flows including FPGA, ASIC, and HLS environments.

Frequently Asked Questions

What are the key features of SystemVerilog that enhance advanced digital design compared to traditional Verilog?

SystemVerilog extends traditional Verilog by adding features such as enhanced data types, object-oriented programming support, assertions, and constrained random stimulus generation. These capabilities facilitate more efficient and robust modeling, verification, and design of complex digital systems.

How does parameterized module design in Verilog improve scalability in advanced digital circuits?

Parameterized modules allow designers to create reusable and configurable components by defining parameters that can be adjusted during instantiation. This promotes scalability and flexibility, enabling the same module to adapt to different bit-widths, configurations, or functionalities without rewriting code.

What is the significance of clock domain crossing (CDC) in advanced Verilog designs, and how can it be handled?

Clock domain crossing occurs when signals transfer between different clock domains, potentially causing metastability issues. In advanced Verilog designs, handling CDC correctly is crucial to ensure data integrity and reliable operation. Techniques such as synchronizer flip-flops, FIFO buffers, and handshake protocols are commonly used to

manage CDC.

How can assertions in SystemVerilog be used to improve verification in advanced digital design?

Assertions in SystemVerilog allow designers to specify expected behavior and constraints directly within the design code. They enable early detection of design errors and functional bugs during simulation and formal verification, improving the robustness and reliability of advanced digital systems.

What role do interfaces play in SystemVerilog for managing complex inter-module communication?

Interfaces in SystemVerilog group related signals and functionality into a single, reusable unit, simplifying module connections and enhancing code readability. They help manage complex inter-module communication by encapsulating handshake protocols, buses, and signal groups, reducing wiring errors and improving design modularity.

How can advanced Verilog techniques optimize FPGA resource utilization and performance?

Advanced Verilog techniques such as pipelining, resource sharing, and hierarchical design help optimize FPGA resource utilization and performance. Using generate statements, parameterization, and efficient coding styles enables designers to tailor hardware implementation, reduce logic duplication, and improve timing closure.

Additional Resources

1. *Advanced Digital Design with the Verilog HDL*
This book delves deeply into complex digital design concepts using Verilog HDL. It covers advanced modeling techniques, synthesis, and verification methodologies. Readers will find comprehensive examples and case studies that illustrate practical applications in FPGA and ASIC design.

2. *Verilog HDL Synthesis: A Practical Primer*
Focused on synthesis, this book guides readers through the intricacies of converting Verilog code into optimized hardware. It emphasizes design constraints, timing analysis, and optimization strategies for high-performance digital circuits. Suitable for engineers looking to bridge the gap between RTL coding and physical hardware implementation.

3. *SystemVerilog for Design: A Guide to Using SystemVerilog for Hardware Design and Modeling*
This book introduces SystemVerilog as an extension of Verilog, offering powerful features for advanced digital design. It covers object-oriented design, assertions, and constrained random verification techniques. The text balances theoretical concepts with practical examples to enhance hardware modeling skills.

4. *Digital Design Using Verilog: Coding for Efficiency, Portability, and Scalability*
Emphasizing clean and efficient coding practices, this book teaches how to write portable and scalable Verilog code. It explores design patterns, modularity, and parameterization to handle complex digital systems. Readers will learn to create designs that are easy to maintain and extend.

5. *High-Level Synthesis Blue Book: From Algorithm to Digital Circuit*
This book explores high-level synthesis techniques using Verilog and SystemVerilog. It guides readers through transforming algorithms into synthesizable RTL code, focusing on design automation and optimization. It is ideal for designers looking to elevate their abstraction level in digital design.

6. *Practical Verification of System-on-Chip Designs*
A comprehensive resource on advanced verification methodologies using Verilog and SystemVerilog. It covers simulation, assertion-based verification, coverage analysis, and formal methods. The book is tailored for engineers involved in verifying complex SoC architectures.

7. *FPGA Design and Implementation Using Verilog*
This book focuses on FPGA-centric design techniques with Verilog HDL. It addresses device architecture, timing closure, and resource optimization specific to FPGA platforms. Practical examples guide readers through implementing high-performance digital systems on FPGAs.

8. *Design and Verification of Digital Systems: Using SystemVerilog*
Combining design and verification, this book provides a thorough treatment of digital system development using SystemVerilog. It covers testbench architecture, UVM methodology, and coverage-driven verification strategies. Readers gain insight into building robust hardware designs with comprehensive test environments.

9. *Low-Power Digital Design with Verilog HDL*
This book addresses power-aware design techniques in Verilog for modern digital circuits. It discusses clock gating, power gating, and dynamic voltage scaling methods to reduce power consumption. Targeted at designers aiming to optimize energy efficiency without sacrificing performance.

Verilog For Advanced Digital Design

verilog for advanced digital design: Advanced Digital Design with the Verilog HDL
Michael D. Ciletti, 2011 This title builds on the student's background from a first course in logic design and focuses on developing, verifying, and synthesizing designs of digital circuits. The Verilog language is introduced in an integrated, but selective manner, only as needed to support design examples.

verilog for advanced digital design: Advanced Digital Design with the Verilog HDL Michael D. Ciletti, 2003

verilog for advanced digital design: Advanced Digital Design with the Verilog HDL Michael D. Ciletti, 2002-08 Accompanying CD-ROM contains the Silos-III Verilog design environment and simulator and the Xilinx integrated synthesis environment (ISE) synthesis tool for FPGAs.

verilog for advanced digital design: *Advanced Digital System Design* Shirshendu Roy, 2023-09-25 The book is designed to serve as a textbook for courses offered to undergraduate and graduate students enrolled in electrical, electronics, and communication engineering. The objective of this book is to help the readers to understand the concepts of digital system design as well as to motivate the students to pursue research in this field. Verilog Hardware Description Language (HDL) is preferred in this book to realize digital architectures. Concepts of Verilog HDL are discussed in a separate chapter and many Verilog codes are given in this book for better understanding. Concepts of system Verilog to realize digital hardware are also discussed in a separate chapter. The book covers basic topics of digital logic design like binary number systems, combinational circuit design, sequential circuit design, and finite state machine (FSM) design. The book also covers some advanced topics on digital arithmetic like design of high-speed adders, multipliers, dividers, square root circuits, and CORDIC block. The readers can learn about FPGA and ASIC implementation steps and issues that arise at the time of implementation. One chapter of the book is dedicated to study the low-power design techniques and another to discuss the concepts of static time analysis (STA) of a digital system. Design and implementation of many digital systems are discussed in detail in a separate chapter. In the last chapter, basics of some advanced FPGA design techniques like partial re-configuration and system on chip (SoC) implementation are discussed. These designs can help the readers to design their architecture. This book can be very helpful to both undergraduate and postgraduate students and researchers.

verilog for advanced digital design: Principles of Verilog Digital Design Wen-Long Chin, 2022-02-27 Covering both the fundamentals and the in-depth topics related to Verilog digital design, both students and experts can benefit from reading this book by gaining a comprehensive understanding of how modern electronic products are designed and implemented. Principles of Verilog Digital Design contains many hands-on examples accompanied by RTL codes that together can bring a beginner into the digital design realm without needing too much background in the subject area. This book has a particular focus on how to transform design concepts into physical implementations using architecture and timing diagrams. Common mistakes a beginner or even an experienced engineer can make are summarized and addressed as well. Beyond the legal details of Verilog codes, the book additionally presents what uses Verilog codes have through some pertinent design principles. Moreover, students reading this book will gain knowledge about system-level design concepts. Several ASIC designs are illustrated in detail as well. In addition to design principles and skills, modern design methodology and how it is carried out in practice today are explored in depth as well.

verilog for advanced digital design: FSM-based Digital Design using Verilog HDL Peter Minns, Ian Elliott, 2008-04-30 As digital circuit elements decrease in physical size, resulting in increasingly complex systems, a basic logic model that can be used in the control and design of a range of semiconductor devices is vital. Finite State Machines (FSM) have numerous advantages; they can be applied to many areas (including motor control, and signal and serial data identification to name a few) and they use less logic than their alternatives, leading to the development of faster digital hardware systems. This clear and logical book presents a range of novel techniques for the rapid and reliable design of digital systems using FSMs, detailing exactly how and where they can be implemented. With a practical approach, it covers synchronous and asynchronous FSMs in the design of both simple and complex systems, and Petri-Net design techniques for sequential/parallel control systems. Chapters on Hardware Description Language cover the widely-used and powerful Verilog HDL in sufficient detail to facilitate the description and verification of FSMs, and FSM based systems, at both the gate and behavioural levels. Throughout, the text incorporates many real-world

examples that demonstrate designs such as data acquisition, a memory tester, and passive serial data monitoring and detection, among others. A useful accompanying CD offers working Verilog software tools for the capture and simulation of design solutions. With a linear programmed learning format, this book works as a concise guide for the practising digital designer. This book will also be of importance to senior students and postgraduates of electronic engineering, who require design skills for the embedded systems market.

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for undergraduate and graduate students in electronics engineering and computer science engineering, Digital VLSI Design Problems and Solution with Verilogalso has a place on the bookshelves of academic researchers and private industry professionals in these fields.

verilog for advanced digital design: FPGA Prototyping by SystemVerilog Examples Pong P. Chu, 2018-05-30 A hands-on introduction to FPGA prototyping and SoC design This is the successor edition of the popular FPGA Prototyping by Verilog Examples text. It follows the same “learning-by-doing” approach to teach the fundamentals and practices of HDL synthesis and FPGA prototyping. The new edition uses a coherent series of examples to demonstrate the process to develop sophisticated digital circuits and IP (intellectual property) cores, integrate them into an SoC (system on a chip) framework, realize the system on an FPGA prototyping board, and verify the hardware and software operation. The examples start with simple gate-level circuits, progress gradually through the RT (register transfer) level modules, and lead to a functional embedded system with custom I/O peripherals and hardware accelerators. Although it is an introductory text, the examples are developed in a rigorous manner, and the derivations follow the strict design guidelines and coding practices used for large, complex digital systems. The book is completely updated and uses the SystemVerilog language, which “absorbs” the Verilog language. It presents the hardware design in the SoC context and introduces the hardware-software co-design concept. Instead of treating examples as isolated entities, the book integrates them into a single coherent SoC platform that allows readers to explore both hardware and software “programmability” and develop complex and interesting embedded system projects. The new edition: Adds four general-purpose IP cores, which are multi-channel PWM (pulse width modulation) controller, I2C controller, SPI controller, and XADC (Xilinx analog-to-digital converter) controller. Introduces a music synthesizer constructed with a DDFS (direct digital frequency synthesis) module and an ADSR (attack-decay-sustain-release) envelope generator. Expands the original video controller into a complete stream based video subsystem that incorporates a video synchronization circuit, a test-pattern generator, an OSD (on-screen display) controller, a sprite generator, and a frame buffer. Provides a detailed discussion on blocking and nonblocking statements and coding styles. Describes basic concepts of software-hardware co-design with Xilinx MicroBlaze MCS soft-core processor. Provides an overview of bus interconnect and interface circuit. Presents basic embedded system software development. Suggests additional modules and peripherals for interesting and challenging projects. FPGA Prototyping by SystemVerilog Examples makes a natural companion text for introductory and advanced digital design courses and embedded system courses. It also serves as an ideal self-teaching guide for practicing engineers who wish to learn more about this emerging area of interest.

verilog for advanced digital design: DIGITAL HARDWARE MODELLING USING SYSTEMVERILOG BATRA, S.B., 2025-05-01 This book offers a practical, application-oriented introduction to Digital Hardware Modelling using SystemVerilog. Written in a student-friendly style adopting a step-by-step learning approach, the book simplifies the nuances of language constructs and design methodologies, empowering readers to design Application Specific Integrated Circuits (ASICs), System on Chip (SoC), and Central Processing Unit (CPU) architectures. It covers a broad spectrum of topics, including SystemVerilog assertions, functional coverage, interfaces, mailboxes, and various data types—presented with clarity and supported by easy-to-follow examples. Authored by an experienced professor and practitioner of ASIC/SoC/CPU and FPGA design, this book is grounded in hands-on experience and real-world application. The extensive coding examples demonstrate using a wide range of SystemVerilog constructs, making this a valuable reference for tackling complex, multi-million-gate ASIC design challenges. It serves as a comprehensive guide for students, educators, and professionals who want to master the SystemVerilog language and apply it in real-world VLSI design environments. Overall, the book helps readers understand the role of modelling in chip fabrication. KEY FEATURES • Covers every aspect of SystemVerilog, from introducing Modelling and SystemVerilog Hardware Description Language to Modelling a Processor in SystemVerilog. • Includes several coding examples to help students to model different digital

hardware. • Covers the concepts of data path and control path, frequently used in processor chips. • Explains the concept of pipelining, used in the processor. TARGET AUDIENCE • B.Tech Electronics, Electronics and Communication Engineering • B.Tech Computer Science and Computer Applications • Front-End Engineers.

verilog for advanced digital design: Advanced VLSI Design and Testability Issues Suman Lata Tripathi, Sobhit Saxena, Sushanta Kumar Mohapatra, 2020-08-19 This book facilitates the VLSI-interested individuals with not only in-depth knowledge, but also the broad aspects of it by explaining its applications in different fields, including image processing and biomedical. The deep understanding of basic concepts gives you the power to develop a new application aspect, which is very well taken care of in this book by using simple language in explaining the concepts. In the VLSI world, the importance of hardware description languages cannot be ignored, as the designing of such dense and complex circuits is not possible without them. Both Verilog and VHDL languages are used here for designing. The current needs of high-performance integrated circuits (ICs) including low power devices and new emerging materials, which can play a very important role in achieving new functionalities, are the most interesting part of the book. The testing of VLSI circuits becomes more crucial than the designing of the circuits in this nanometer technology era. The role of fault simulation algorithms is very well explained, and its implementation using Verilog is the key aspect of this book. This book is well organized into 20 chapters. Chapter 1 emphasizes on uses of FPGA on various image processing and biomedical applications. Then, the descriptions enlighten the basic understanding of digital design from the perspective of HDL in Chapters 2–5. The performance enhancement with alternate material or geometry for silicon-based FET designs is focused in Chapters 6 and 7. Chapters 8 and 9 describe the study of bimolecular interactions with biosensing FETs. Chapters 10–13 deal with advanced FET structures available in various shapes, materials such as nanowire, HFET, and their comparison in terms of device performance metrics calculation. Chapters 14–18 describe different application-specific VLSI design techniques and challenges for analog and digital circuit designs. Chapter 19 explains the VLSI testability issues with the description of simulation and its categorization into logic and fault simulation for test pattern generation using Verilog HDL. Chapter 20 deals with a secured VLSI design with hardware obfuscation by hiding the IC’s structure and function, which makes it much more difficult to reverse engineer.

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developers and newcomers aspiring to excel in the dynamic field of digital design and simulation.

verilog for advanced digital design: FPGA Prototyping by VHDL Examples Pong P. Chu, 2018-01-25 A hands-on introduction to FPGA prototyping and SoC design This Second Edition of the popular book follows the same “learning-by-doing” approach to teach the fundamentals and practices of VHDL synthesis and FPGA prototyping. It uses a coherent series of examples to demonstrate the process to develop sophisticated digital circuits and IP (intellectual property) cores, integrate them into an SoC (system on a chip) framework, realize the system on an FPGA prototyping board, and verify the hardware and software operation. The examples start with simple gate-level circuits, progress gradually through the RT (register transfer) level modules, and lead to a functional embedded system with custom I/O peripherals and hardware accelerators. Although it is an introductory text, the examples are developed in a rigorous manner, and the derivations follow strict design guidelines and coding practices used for large, complex digital systems. The new edition is completely updated. It presents the hardware design in the SoC context and introduces the hardware-software co-design concept. Instead of treating examples as isolated entities, the book integrates them into a single coherent SoC platform that allows readers to explore both hardware and software “programmability” and develop complex and interesting embedded system projects. The revised edition: Adds four general-purpose IP cores, which are multi-channel PWM (pulse width modulation) controller, I2C controller, SPI controller, and XADC (Xilinx analog-to-digital converter) controller. Introduces a music synthesizer constructed with a DDFS (direct digital frequency synthesis) module and an ADSR (attack-decay-sustain-release) envelop generator. Expands the original video controller into a complete stream-based video subsystem that incorporates a video synchronization circuit, a test pattern generator, an OSD (on-screen display) controller, a sprite generator, and a frame buffer. Introduces basic concepts of software-hardware co-design with Xilinx MicroBlaze MCS soft-core processor. Provides an overview of bus interconnect and interface circuit. Introduces basic embedded system software development. Suggests additional modules and peripherals for interesting and challenging projects. The FPGA Prototyping by VHDL Examples, Second Edition makes a natural companion text for introductory and advanced digital design courses and embedded system course. It also serves as an ideal self-teaching guide for practicing engineers who wish to learn more about this emerging area of interest.

verilog for advanced digital design: *Digital Design and Computer Architecture* David Harris, Sarah Harris, 2010-07-26 Digital Design and Computer Architecture is designed for courses that combine digital logic design with computer organization/architecture or that teach these subjects as a two-course sequence. Digital Design and Computer Architecture begins with a modern approach by rigorously covering the fundamentals of digital logic design and then introducing Hardware Description Languages (HDLs). Featuring examples of the two most widely-used HDLs, VHDL and Verilog, the first half of the text prepares the reader for what follows in the second: the design of a MIPS Processor. By the end of Digital Design and Computer Architecture, readers will be able to build their own microprocessor and will have a top-to-bottom understanding of how it works--even if they have no formal background in design or architecture beyond an introductory class. David Harris and Sarah Harris combine an engaging and humorous writing style with an updated and hands-on approach to digital design. - Unique presentation of digital logic design from the perspective of computer architecture using a real instruction set, MIPS. - Side-by-side examples of the two most prominent Hardware Design Languages--VHDL and Verilog--illustrate and compare the ways the each can be used in the design of digital systems. - Worked examples conclude each section to enhance the reader's understanding and retention of the material.

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