advanced verilog hdl design

advanced verilog hdl design represents a critical skill set in the development of complex digital systems and integrated circuits. As digital technology continues to evolve rapidly, mastering advanced concepts in Verilog Hardware Description Language (HDL) design becomes essential for engineers seeking to implement sophisticated logic on FPGAs and ASICs. This article explores the core principles, methodologies, and best practices that define advanced Verilog HDL design, highlighting techniques such as parameterization, hierarchical modeling, testbench automation, and timing optimization. Emphasis is placed on how these practices contribute to efficient, scalable, and maintainable hardware descriptions. Additionally, the discussion covers the integration of assertion-based verification and low-power design strategies to meet modern design requirements. The comprehensive overview provided here aims to equip professionals with the insights necessary to elevate their Verilog projects to industry standards. The following sections break down these topics in detail, forming a structured guide to advanced Verilog HDL design.

Understanding Advanced Verilog HDL Constructs

Advanced Verilog HDL design begins with a comprehensive understanding of the language’s sophisticated constructs beyond basic gate-level descriptions. These constructs allow designers to express complex behavior efficiently and with high readability. Key elements include parameterized modules, generate statements, and system tasks that facilitate reusable and scalable designs.

Parameterized Modules

Parameterized modules enable designers to create flexible hardware blocks that can be customized by passing parameters during instantiation. This approach reduces code duplication and improves maintainability by allowing

the same module to adapt to different data widths or configurations.

- Use of *parameter* and *localparam* keywords
- Allowing variation in bus widths and depths
- Supporting multiple configurations through a single module definition

Generate Statements

The *generate* construct supports conditional and iterative instantiation of hardware components within a design. It is essential for creating parameter-dependent structures such as arrays of registers or complex interconnects, streamlining the creation of repetitive logic blocks.

System Tasks and Functions

System tasks like *$display* and *$finish*, along with user-defined functions, provide mechanisms for debugging, simulation control, and encapsulating reusable code snippets. These tools are vital for complex design verification and simulation management.

Hierarchical and Modular Design Techniques

Hierarchical design is a cornerstone of advanced Verilog HDL development, promoting clarity, reusability, and efficient management of large designs. Modularization involves breaking down the system into smaller, manageable blocks with well-defined interfaces.

Module Instantiation and Connectivity

Instantiating modules within parent designs allows for hierarchical organization. Designers must carefully define input and output ports and use named port mapping to avoid errors and enhance readability.

Interface Abstraction

Abstraction of interfaces using constructs like *interfaces* or bus macros simplifies the connectivity between modules and eases integration. This technique reduces wiring complexity and enhances design portability.

Design Reuse Strategies

Reusable design components contribute significantly to development efficiency. By creating parameterized and well-documented modules, designers foster portability and adaptability across multiple projects, which is essential in professional environments.

Testbench Development and Verification Strategies

Robust verification methodologies are critical in advanced Verilog HDL design to ensure functional correctness and performance compliance. Developing comprehensive testbenches and employing verification techniques help detect and correct design flaws early.

Self-Checking Testbenches

Self-checking testbenches automate the validation process by incorporating stimulus generation, response monitoring, and pass/fail decision logic. This automation reduces manual intervention and speeds up verification cycles.

Randomized Testing and Coverage

Randomized stimulus generation combined with coverage analysis ensures exhaustive testing of corner cases. This technique improves confidence in design robustness and helps identify untested scenarios.

Use of Verification Languages and Methodologies

Integration of SystemVerilog features and methodologies like UVM (Universal Verification Methodology) enhances the verification process, although traditional Verilog testbenches can also implement advanced verification concepts.

Timing Analysis and Optimization

Effective timing analysis and optimization are indispensable for meeting performance goals in advanced Verilog HDL design. Understanding timing constraints, clock domain crossing, and synthesis implications allows designers to optimize critical paths and ensure reliable operation.

Setup and Hold Time Considerations

Ensuring that data signals meet setup and hold timing requirements relative to clock edges is fundamental. Violations can cause metastability and unpredictable behavior, which must be addressed during design and verification.

Clock Domain Crossing Techniques

Designs often include multiple asynchronous clock domains. Proper synchronization techniques such as using synchronizer flip-flops and FIFOs prevent data corruption and timing hazards between these domains.

Optimization Strategies

Reducing logic depth, balancing pipeline stages, and leveraging synthesis directives help optimize timing. Designers should also analyze critical paths and apply retiming or resource sharing where appropriate.

Low-Power Design Approaches in Verilog

Power efficiency is increasingly important in modern digital designs. Advanced Verilog HDL design incorporates strategies to minimize power consumption without sacrificing performance or functionality.

Clock Gating

Clock gating disables the clock signal to idle modules, reducing dynamic power consumption. Implementing clock gating at the RTL level requires careful control logic to avoid timing glitches.

Power-Aware Coding Practices

Writing RTL code that minimizes switching activity, such as avoiding unnecessary toggling of signals and optimizing finite state machines, contributes to lower power usage.

Multi-Voltage and Power Domains

Partitioning designs into multiple power domains allows selective power gating and voltage scaling. Verilog constructs can model these domains to support low-power verification flows.

Assertion-Based Verification and Debugging

Assertion-based verification (ABV) is an advanced technique that embeds formal checks within the RTL code to detect protocol violations and functional errors during simulation and formal verification.

SystemVerilog Assertions (SVA)

SystemVerilog Assertions provide a powerful framework for specifying design behavior properties, enabling automatic detection of incorrect behavior and improving debugging efficiency.

Embedding Assertions in Verilog Designs

While traditional Verilog has limited assertion support, advanced designs integrate SystemVerilog or vendor-specific assertion languages to leverage ABV benefits fully.

Debugging with Assertions

Assertions help isolate faults early by providing immediate feedback when conditions are violated, thus reducing time spent on root cause analysis and improving overall design quality.

Frequently Asked Questions

What are the key features of advanced Verilog HDL design?

Advanced Verilog HDL design includes features such as parameterized modules, generate statements for code reuse, system tasks for simulation control, assertions for verification, and support for complex data types and interfaces.

How does parameterization improve Verilog HDL design?

Parameterization allows designers to create flexible and reusable modules by defining generic parameters that can be adjusted during module instantiation, reducing code duplication and enhancing scalability.

What is the role of 'generate' statements in advanced Verilog?

Generate statements enable conditional and iterative code generation at compile time, allowing designers to create multiple instances of modules or logic blocks efficiently based on parameters or constants.

How are assertions used in advanced Verilog HDL for verification?

Assertions in Verilog (using SystemVerilog assertions) help verify design correctness by checking that certain conditions hold true during simulation, facilitating early detection of design errors and improving robustness.

What techniques are used in advanced Verilog to handle complex state machines?

Advanced techniques include encoding states with enumerated types, using one-hot or gray code encoding for efficiency, modularizing state machine logic, and employing formal verification to ensure correctness.

How does clock domain crossing (CDC) affect advanced Verilog design?

CDC requires careful design techniques such as synchronization registers, FIFO buffers, and metastability mitigation to ensure reliable data transfer between different clock domains in advanced Verilog designs.

What is the significance of interfaces and modports in advanced Verilog?

Interfaces and modports encapsulate signal groups and define directional access, improving modularity, readability, and maintainability of complex designs by abstracting communication between modules.

How does advanced Verilog HDL support low-power design methodologies?

Advanced Verilog supports low-power design through constructs like power gating, clock gating, and multi-voltage domain modeling, enabling designers to implement power-saving techniques effectively.

What are some best practices for writing synthesizable advanced Verilog code?

Best practices include avoiding delays and non-synthesizable constructs,

using proper coding styles for combinational and sequential logic, employing parameterization and generate blocks for scalability, and thorough simulation and synthesis tool checks.

Additional Resources

1. *Advanced Digital Design with the Verilog HDL*
This book delves into sophisticated design techniques using Verilog HDL, focusing on real-world applications and best practices. It covers topics such as timing analysis, synthesis optimization, and design for testability. Ideal for engineers looking to deepen their understanding of complex digital system design.

2. *Verilog HDL Synthesis: A Practical Primer*
A comprehensive guide that bridges the gap between Verilog coding and hardware synthesis. The book explains synthesis constraints, coding styles for efficient synthesis, and how to avoid common pitfalls. It is essential for designers aiming to write synthesizable and optimized Verilog code.

3. *FPGA Prototyping by Verilog Examples: Xilinx Spartan-3 Version*
This hands-on book uses practical examples to teach advanced Verilog design concepts on FPGA platforms. It covers topics such as finite state machines, datapath design, and interfacing with peripherals. Readers gain valuable experience in prototyping and debugging complex designs.

4. *Effective Verilog: Coding, Debugging, and Testing*
Focused on improving coding practices, this book provides techniques for writing clean, maintainable, and efficient Verilog code. It also discusses advanced debugging methods and testing strategies, including testbenches and assertion-based verification. It is perfect for designers seeking to enhance code quality and reliability.

5. *SystemVerilog for Design: A Guide to Using SystemVerilog for Hardware Design and Modeling*
While primarily about SystemVerilog, this book covers advanced features that extend traditional Verilog capabilities. It explores design and modeling techniques that improve productivity and design robustness. The book is suitable for designers transitioning to SystemVerilog from Verilog.

6. *Digital Design and Verilog HDL Fundamentals*
This text offers a blend of digital design theory and practical Verilog HDL implementation. It covers combinational and sequential logic design, timing analysis, and advanced synthesis topics. Ideal for readers wanting a solid foundation coupled with advanced design insights.

7. *High-Level Synthesis Blue Book: From Algorithm to Digital Circuit*
This book focuses on high-level synthesis (HLS) using Verilog as the target HDL. It explains how to convert algorithms into efficient hardware descriptions, emphasizing optimization and verification. It is a valuable resource for designers integrating HLS into their Verilog design flow.

8. *Design Recipes for FPGAs: Using Verilog and VHDL*
Containing practical "recipes," this book addresses advanced design challenges with step-by-step Verilog solutions. Topics include complex state machines, pipelining, and memory interfacing. It's an excellent reference for engineers tackling real-world FPGA design problems.

9. *Modeling and Verification of Real-Time Systems Using Verilog*
This book explores the use of Verilog for modeling and verifying real-time and embedded systems. It discusses timing constraints, concurrency, and formal verification techniques tailored to advanced Verilog designs. Suitable for professionals working on time-critical hardware applications.

Advanced Verilog Hdl Design

advanced verilog hdl design: Advanced Digital Design with the Verilog HDL Micahel, D. Ciletti, For an advanced course in digital design for seniors and first-year graduate students in electrical engineering, computer engineering and computer science. This book builds on the student's background from a first course in logic design and focuses on developing, verifying and synthesizing designs of digital circuits. The Verilog language is introduced in an integrated, but selective manner, only as needed to support design examples (includes appendices for additional language details). It addresses the design of several important circuits used in computer systems, digital signal processing, image processing and other applications.

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advanced verilog hdl design: Verilog HDL Samir Palnitkar, 2003 VERILOG HDL, Second Editionby Samir PalnitkarWith a Foreword by Prabhu GoelWritten forboth experienced and new users, this book gives you broad coverage of VerilogHDL. The book stresses the practical design and verification perspective ofVerilog rather than emphasizing only the language aspects. The informationpresented is fully compliant with the IEEE 1364-2001 Verilog HDL standard. Among its many features, this edition- bull; bull;Describes state-of-the-art verification methodologies bull;Provides full coverage of gate, dataflow (RTL), behavioral and switch modeling bull;Introduces you to the Programming Language Interface (PLI) bull;Describes logic synthesis methodologies bull;Explains timing and delay simulation bull;Discusses user-defined primitives bull;Offers many practical modeling tips Includes over 300 illustrations, examples, and exercises, and a Verilog resource list.Learning objectives and summaries are provided for each chapter. About the CD-ROMThe CD-ROM contains a Verilog simulator with agraphical user interface and the source code for the examples in the book. Whatpeople are saying about Verilog HDL- Mr.Palnitkar illustrates how and why Verilog HDL is used to develop today'smost complex digital designs. This book is valuable to both the novice and theexperienced Verilog user. I highly recommend it to anyone exploring Verilogbased design. -RajeevMadhavan, Chairman and CEO, Magma Design Automation Thisbook is unique in its breadth of information on Verilog and Verilog-relatedtopics. It is fully compliant with the IEEE 1364-2001 standard, contains allthe information that you need on

the basics, and devotes several chapters toadvanced topics such as verification, PLI, synthesis and modelingtechniques. -MichaelMcNamara, Chair, IEEE 1364-2001 Verilog Standards Organization Thishas been my favorite Verilog book since I picked it up in college. It is theonly book that covers practical Verilog. A must have for beginners andexperts. -BerendOzceri, Design Engineer, Cisco Systems, Inc. Simple,logical and well-organized material with plenty of illustrations, makes this anideal textbook. -Arun K. Somani, Jerry R. Junkins Chair Professor,Department of Electrical and Computer Engineering, Iowa State University, Ames PRENTICE HALL Professional Technical Reference Upper Saddle River, NJ 07458 www.phptr.com ISBN: 0-13-044911-3

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advanced verilog hdl design: Advanced Digital System Design Shirshendu Roy, 2023-09-25 The book is designed to serve as a textbook for courses offered to undergraduate and graduate students enrolled in electrical, electronics, and communication engineering. The objective of this book is to help the readers to understand the concepts of digital system design as well as to motivate the students to pursue research in this field. Verilog Hardware Description Language (HDL) is preferred in this book to realize digital architectures. Concepts of Verilog HDL are discussed in a separate chapter and many Verilog codes are given in this book for better understanding. Concepts of system Verilog to realize digital hardware are also discussed in a separate chapter. The book covers basic topics of digital logic design like binary number systems, combinational circuit design, sequential circuit design, and finite state machine (FSM) design. The book also covers some advanced topics on digital arithmetic like design of high-speed adders, multipliers, dividers, square root circuits, and CORDIC block. The readers can learn about FPGA and ASIC implementation steps and issues that arise at the time of implementation. One chapter of the book is dedicated to study the low-power design techniques and another to discuss the concepts of static time analysis (STA) of a digital system. Design and implementation of many digital systems are discussed in detail in a separate chapter. In the last chapter, basics of some advanced FPGA design techniques like partial re-configuration and system on chip (SoC) implementation are discussed. These designs can help the readers to design their architecture. This book can be very helpful to both undergraduate and postgraduate students and researchers.

advanced verilog hdl design: Advanced VLSI Design and Testability Issues Suman Lata Tripathi, Sobhit Saxena, Sushanta Kumar Mohapatra, 2020-08-18 This book facilitates the VLSI-interested individuals with not only in-depth knowledge, but also the broad aspects of it by explaining its applications in different fields, including image processing and biomedical. The deep understanding of basic concepts gives you the power to develop a new application aspect, which is very well taken care of in this book by using simple language in explaining the concepts. In the VLSI world, the importance of hardware description languages cannot be ignored, as the designing of such dense and complex circuits is not possible without them. Both Verilog and VHDL languages are used here for designing. The current needs of high-performance integrated circuits (ICs) including low power devices and new emerging materials, which can play a very important role in achieving new functionalities, are the most interesting part of the book. The testing of VLSI circuits becomes more crucial than the designing of the circuits in this nanometer technology era. The role of fault simulation algorithms is very well explained, and its implementation using Verilog is the key aspect of this book. This book is well organized into 20 chapters. Chapter 1 emphasizes on uses of FPGA on various image processing and biomedical applications. Then, the descriptions enlighten the basic

understanding of digital design from the perspective of HDL in Chapters 2–5. The performance enhancement with alternate material or geometry for silicon-based FET designs is focused in Chapters 6 and 7. Chapters 8 and 9 describe the study of bimolecular interactions with biosensing FETs. Chapters 10–13 deal with advanced FET structures available in various shapes, materials such as nanowire, HFET, and their comparison in terms of device performance metrics calculation. Chapters 14–18 describe different application-specific VLSI design techniques and challenges for analog and digital circuit designs. Chapter 19 explains the VLSI testability issues with the description of simulation and its categorization into logic and fault simulation for test pattern generation using Verilog HDL. Chapter 20 deals with a secured VLSI design with hardware obfuscation by hiding the IC's structure and function, which makes it much more difficult to reverse engineer.

advanced verilog hdl design: Hardware Description Language Demystified Dr. Cherry Bhargava, Dr. Rajkumar Sarma, 2020-08-27 Get familiar and work with the basic and advanced Modeling types in Verilog HDL Key Features _ Learn about the step-wise process to use Verilog design tools such as Xilinx, Vivado, Cadence NC-SIM _ Explore the various types of HDL and its need _ Learn Verilog HDL modeling types using examples _ Learn advanced concept such as UDP, Switch level modeling _ Learn about FPGA based prototyping of the digital system Description Hardware Description Language (HDL) allows analysis and simulation of digital logic and circuits. The HDL is an integral part of the EDA (electronic design automation) tool for PLDs, microprocessors, and ASICs. So, HDL is used to describe a Digital System. The combinational and sequential logic circuits can be described easily using HDL. Verilog HDL, standardized as IEEE 1364, is a hardware description language used to model electronic systems. This book is a comprehensive guide about the digital system and its design using various VLSI design tools as well as Verilog HDL. The step-wise procedure to use various VLSI tools such as Xilinx, Vivado, Cadence NC-SIM, is covered in this book. It also explains the advanced concept such as User Define Primitives (UDP), switch level modeling, reconfigurable computing, etc. Finally, this book ends with FPGA based prototyping of the digital system. By the end of this book, you will understand everything related to digital system design. What will you learn _ Implement Adder, Subtractor, Adder-Cum-Subtractor using Verilog HDL _ Explore the various Modeling styles in Verilog HDL _ Implement Switch level modeling using Verilog HDL _ Get familiar with advanced modeling techniques in Verilog HDL _ Get to know more about FPGA based prototyping using Verilog HDL Who this book is for Anyone interested in Electronics and VLSI design and want to learn Digital System Design with Verilog HDL will find this book useful. IC developers can also use this book as a quick reference for Verilog HDL fundamentals & features. Table of Contents 1. An Introduction to VLSI Design Tools 2. Need of Hardware Description Language (HDL) 3. Logic Gate Implementation in Verilog HDL 4. Adder-Subtractor Implementation Using Verilog HDL 5. Multiplexer/Demultiplexer Implementation in Verilog HDL 6. Encoder/Decoder Implementation Using Verilog HDL 7. Magnitude Comparator Implementation Using Verilog HDL 8. Flip-Flop Implementation Using Verilog HDL 9. Shift Registers Implementation Using Verilog HDL 10. Counter Implementation Using Verilog HDL 11. Shift Register Counter Implementation Using Verilog HDL 12. Advanced Modeling Techniques 13. Switch Level Modeling 14. FPGA Prototyping in Verilog HDL

advanced verilog hdl design: Principles of Verilog Digital Design Wen-Long Chin, 2022-02-27 Covering both the fundamentals and the in-depth topics related to Verilog digital design, both students and experts can benefit from reading this book by gaining a comprehensive understanding of how modern electronic products are designed and implemented. Principles of Verilog Digital Design contains many hands-on examples accompanied by RTL codes that together can bring a beginner into the digital design realm without needing too much background in the subject area. This book has a particular focus on how to transform design concepts into physical implementations using architecture and timing diagrams. Common mistakes a beginner or even an experienced engineer can make are summarized and addressed as well. Beyond the legal details of Verilog codes, the book additionally presents what uses Verilog codes have through some pertinent

design principles. Moreover, students reading this book will gain knowledge about system-level design concepts. Several ASIC designs are illustrated in detail as well. In addition to design principles and skills, modern design methodology and how it is carried out in practice today are explored in depth as well.

advanced verilog hdl design: Advanced HDL Synthesis and SOC Prototyping Vaibbhav Taraate, 2018-12-15 This book describes RTL design using Verilog, synthesis and timing closure for System On Chip (SOC) design blocks. It covers the complex RTL design scenarios and challenges for SOC designs and provides practical information on performance improvements in SOC, as well as Application Specific Integrated Circuit (ASIC) designs. Prototyping using modern high density Field Programmable Gate Arrays (FPGAs) is discussed in this book with the practical examples and case studies. The book discusses SOC design, performance improvement techniques, testing and system level verification, while also describing the modern Intel FPGA/XILINX FPGA architectures and their use in SOC prototyping. Further, the book covers the Synopsys Design Compiler (DC) and Prime Time (PT) commands, and how they can be used to optimize complex ASIC/SOC designs. The contents of this book will be useful to students and professionals alike.

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Engineering Sciences.

advanced verilog hdl design: DIGITAL HARDWARE MODELLING USING SYSTEMVERILOG BATRA, S.B., 2025-05-01 This book offers a practical, application-oriented introduction to Digital Hardware Modelling using SystemVerilog. Written in a student-friendly style adopting a step-by-step learning approach, the book simplifies the nuances of language constructs and design methodologies, empowering readers to design Application Specific Integrated Circuits (ASICs), System on Chip (SoC), and Central Processing Unit (CPU) architectures. It covers a broad spectrum of topics, including SystemVerilog assertions, functional coverage, interfaces, mailboxes, and various data types—presented with clarity and supported by easy-to-follow examples. Authored by an experienced professor and practitioner of ASIC/SoC/CPU and FPGA design, this book is grounded in hands-on experience and real-world application. The extensive coding examples demonstrate using a wide range of SystemVerilog constructs, making this a valuable reference for tackling complex, multi-million-gate ASIC design challenges. It serves as a comprehensive guide for students, educators, and professionals who want to master the SystemVerilog language and apply it in real-world VLSI design environments. Overall, the book helps readers understand the role of modelling in chip fabrication. KEY FEATURES • Covers every aspect of SystemVerilog, from introducing Modelling and SystemVerilog Hardware Description Language to Modelling a Processor in SystemVerilog. • Includes several coding examples to help students to model different digital hardware. • Covers the concepts of data path and control path, frequently used in processor chips. • Explains the concept of pipelining, used in the processor. TARGET AUDIENCE • B.Tech Electronics, Electronics and Communication Engineering • B.Tech Computer Science and Computer Applications • Front-End Engineers.

advanced verilog hdl design: Digital Design and Verilog HDL Fundamentals Joseph Cavanagh, 2017-12-19 Comprehensive and self contained, this tutorial covers the design of a plethora of combinational and sequential logic circuits using conventional logic design and Verilog HDL. Number systems and number representations are presented along with various binary codes. Several advanced topics are covered, including functional decomposition and iterative networks. A variety of examples are provided for combinational and sequential logic, computer arithmetic, and advanced topics such as Hamming code error correction. Constructs supported by Verilog are described in detail. All designs are continued to completion. Each chapter includes numerous design issues of varying complexity to be resolved by the reader.

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advanced verilog hdl design: *Hardware Description Language Demystified* Dr. Cherry Sarma

Bhargava, Dr. Rajkumar, 2020-09-03 Get familiar and work with the basic and advanced Modeling types in Verilog HDL Key Features a- Learn about the step-wise process to use Verilog design tools such as Xilinx, Vivado, Cadence NC-SIM a- Explore the various types of HDL and its need a- Learn Verilog HDL modeling types using examples a- Learn advanced concept such as UDP, Switch level modeling a- Learn about FPGA based prototyping of the digital system Description Hardware Description Language (HDL) allows analysis and simulation of digital logic and circuits. The HDL is an integral part of the EDA (electronic design automation) tool for PLDs, microprocessors, and ASICs. So, HDL is used to describe a Digital System. The combinational and sequential logic circuits can be described easily using HDL. Verilog HDL, standardized as IEEE 1364, is a hardware description language used to model electronic systems. This book is a comprehensive guide about the digital system and its design using various VLSI design tools as well as Verilog HDL. The step-wise procedure to use various VLSI tools such as Xilinx, Vivado, Cadence NC-SIM, is covered in this book. It also explains the advanced concept such as User Define Primitives (UDP), switch level modeling, reconfigurable computing, etc. Finally, this book ends with FPGA based prototyping of the digital system. By the end of this book, you will understand everything related to digital system design. What will you learn a- Implement Adder, Subtractor, Adder-Cum-Subtractor using Verilog HDL a- Explore the various Modeling styles in Verilog HDL a- Implement Switch level modeling using Verilog HDL a- Get familiar with advanced modeling techniques in Verilog HDL a- Get to know more about FPGA based prototyping using Verilog HDL Who this book is for Anyone interested in Electronics and VLSI design and want to learn Digital System Design with Verilog HDL will find this book useful. IC developers can also use this book as a quick reference for Verilog HDL fundamentals & features. Table of Contents 1. An Introduction to VLSI Design Tools 2. Need of Hardware Description Language (HDL) 3. Logic Gate Implementation in Verilog HDL 4. Adder-Subtractor Implementation Using Verilog HDL 5. Multiplexer/Demultiplexer Implementation in Verilog HDL 6. Encoder/Decoder Implementation Using Verilog HDL 7. Magnitude Comparator Implementation Using Verilog HDL 8. Flip-Flop Implementation Using Verilog HDL 9. Shift Registers Implementation Using Verilog HDL 10. Counter Implementation Using Verilog HDL 11. Shift Register Counter Implementation Using Verilog HDL 12. Advanced Modeling Techniques 13. Switch Level Modeling 14. FPGA Prototyping in Verilog HDL About the Author Dr. Cherry Bhargava is working as an associate professor and head, VLSI domain, School of Electrical and Electronics Engineering at Lovely Professional University, Punjab, India. She has more than 14 years of teaching and research experience. She is Ph.D. (ECE), IKGPTU, M.Tech (VLSI Design & CAD) Thapar University and B.Tech (Electronics and Instrumentation) from Kurukshetra University. She is GATE qualified with All India Rank 428. She has authored about 50 technical research papers in SCI, Scopus indexed quality journals, and national/international conferences. She has eleven books related to reliability, artificial intelligence, and digital electronics to her credit. She has registered five copyrights and filed twenty-two patents. Your LinkedIn Profile https://in.linkedin.com/in/dr-cherry-bhargava-7315619 Dr. Rajkumar Sarma received his B.E. in Electronics and Communications Engineering from Vinayaka Mission's University, Salem, India & M.Tech degree from Lovely Professional University, Phagwara, Punjab and currently pursuing Ph.D. from Lovely Professional University, Phagwara, Punjab. Your LinkedIn Profile www.linkedin.com/in/rajkumar-sarma-213657126

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